



Announcement and Invitation
A FREE DISTINGUISHED LECTURE

ON

*Breaking the 3D power delivery walls
using voltage stacking*

by

IEEE CAS Distinguished Lecturer



Prof. Dr. Mircea Stan

University of Virginia
IEEE Fellow

**15th December 2014 (Monday)
9.00 AM – 1.00 PM**

**Seminar Room,
Level 2 Administration Building,
Faculty of Engineering, UPM, 43400 Serdang Selangor**

Sponsored by the IEEE Circuits and Systems Society under Distinguished Lecturer Program

Abstract:

The power delivery walls include: power density (power consumption density increases beyond the heat dissipation capabilities of the technology), power and ground power delivery pins (chip power consumption requires increasing numbers of pins), 3DIC power density (physical stacking in the third dimension exacerbates the two-dimensional explosion), on-chip power regulation efficiency (relatively poor efficiencies achievable with on-chip regulators limit the effectiveness of many low power schemes). In this talk we demonstrate how voltage stacking is a comprehensive method for addressing the power delivery walls above, with special emphasis on 3DIC.

Biography:

Mircea R. Stan received the Ph.D. and M.S. degrees in Electrical and Computer Engineering from the University of Massachusetts at Amherst and the Diploma in Electronics and Communications from "Politehnica" University in Bucharest, Romania. Since 1996 he has been with the Department of Electrical and Computer Engineering at the University of Virginia, where he is now a professor. Prof. Stan is teaching and doing research in the areas of high-performance low-power VLSI, temperature-aware circuits and architecture, embedded systems, and nanoelectronics. He has more than eight years of industrial experience and 16 years of academic experience, has been a visiting faculty at UC Berkeley in 2004-2005, at IBM in 2000, and at Intel in 2002 and 1999. He has received the NSF CAREER award in 1997 and was a co-author on best paper awards at ISQED 2008, GLSVLSI 2006, ISCA 2003 and SHAMAN 2002. He was the chair of the VLSI Systems and Applications Technical Committee (VSA-TC) of IEEE CAS in 2005-2007, general chair for ISLPED 2006 and GLSVLSI 2004, TPC chair for NanoNets 2007 and ISLPED 2005 and a Distinguished Lecturer for IEEE SSCS in 2007-2008, and for IEEE CAS in 2004-2005.

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